

What is claimed is:

1. A device for electrostatic discharge input protection comprising:  
a transistor with gate, source, drain and substrate terminals;  
an input signal terminal coupled to said source terminal of said transistor;  
a reference point coupled to said gate and substrate terminals of said transistor; and  
an output signal terminal coupled to said drain terminal of said transistor;  
where the leakage current of said transistor is reduced to a sub-threshold level while an increasing source voltage applied at said source terminal reduces the gate-to-source voltage and reduces its threshold voltage.
2. The device of claim 1 wherein said reference point comprises the ground for a specific electrostatic discharge application.
3. The device of claim 1 wherein said reference point is 0 volts.
4. The device of claim 1 wherein said reference point comprises  $V_{SS}$ .
5. The device of claim 1 wherein said source voltage is a few 100mV.
6. The device of claim 5 wherein said leakage current is approximately  $10^{-14}$  A/ $\mu$ m.
7. The device of claim 1 wherein said transistor is an NMOS transistor.
8. The device of claim 1 wherein said transistor is a PMOS transistor.

1 9. A low leakage Electrostatic Discharge (ESD) protection scheme  
2 comprising:  
3 a plurality of low operating voltage devices, each device having at least  
4 one device input for receiving an input signal;  
5 a plurality of input terminals for coupling an input signal to a device via a  
6 corresponding device input;  
7 a plurality of transistors with gate, substrate, source and drain terminals,  
8 each transistor providing an alternate pathway via a source terminal for signals  
9 from said plurality of input terminals; and  
10 a reference coupled to corresponding gate and substrate terminals of said  
11 plurality of input protection transistors; and  
12 a source voltage driving both said source terminals of said input protection  
13 transistors and said inputs of said low operating voltage devices;  
14 wherein ESD protection is achieved by coupling the source terminals of  
15 said plurality of transistors to said plurality of input terminals thereby limiting the  
16 leakage current of each of said transistors to a sub-threshold level even as said  
17 source voltage increases.

1 10. The protection scheme of claim 9 wherein said plurality of low operating  
2 voltage devices are CMOS.

1 11. The protection scheme of claim 9 wherein said reference point comprises  
2 a ground reference.

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12. The protection scheme of claim 9 wherein said reference point is 0 volts.

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13. The protection scheme of claim 9 wherein said reference point comprises  $V_{SS}$  for said low voltage operating devices and said plurality of transistors.

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14. The protection scheme of claim 9 wherein said source voltage is limited to a few 100mV.

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15. The protection scheme of claim 14 wherein the resulting leakage current from said source voltage is approximately  $10^{-14}$  A/ $\mu$ m.

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16. The protection scheme of claim 9 wherein said plurality of transistors are NMOS type.

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17. The protection scheme of claim 9 wherein said plurality of transistors are PMOS type.

1 18. A low voltage Integrated Circuit (IC) with on-board ESD input protection  
2 comprising:

3 a plurality of low operating voltage devices,  
4 at least one reference point, one supply voltage point and a plurality of  
5 input terminals coupled to said devices;

6 a plurality of input paths for coupling input signals to said devices via said  
7 input terminals; and

8 a plurality of input protection transistors with gate, substrate, source, and  
9 drain terminals arranged between said input paths and said devices, each  
10 source terminal coupled to a corresponding input path, each gate and substrate  
11 terminal coupled to a reference point;

12 wherein a leakage current of said input protection transistors is controlled  
13 to a sub-threshold level over a range of voltages applied to each source terminal  
14 of said input protection transistors.

1 19. The IC of claim 18 wherein said plurality of input protection transistors are  
2 NMOS type.

1 20. The IC of claim 18 wherein said plurality of input protection transistors are  
2 PMOS type.

1 21. The IC of claim 18 wherein said devices, terminals, input paths, and input  
2 protection transistors are contained on a single semiconductor chip.

1 22. The IC of claim 18 wherein said reference point is a ground reference  
2 point associated with said devices.

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24. The IC of claim 18 wherein said reference point is tied to said  $V_{SS}$ .